F.PORT PROTOCOL (without PhyId) V2.1

F.Port is an interface between receiver and other parts connected to the receiver for data transaction, e.g. receiver and servos, or receiver and a sensor. F.Port is a one line bus with one master and several slaves. Control channels, downlink data, and uplink data are included on the BUS. It has higher speed (115200bit/s) than S.Port.

1. Physical Definition

Tri-State TTL is implemented as communication level, 2.5v/3.3V as digit “0”, 0V as digit “1”, the voltage between 1V and 2V is not distinguished. In multi-device condition, the transmitter should put its output to tristate when not transmitting. In two device condition, two device can connect by separate rxd/txd wire-pares.

Serial port is introduced to send/receive data bytes.

Serial port definition: 115200bps, No Parity, 8bits data, 1 stopping-bit.

2. Frame Definition

There are 3 types of frames: control frame, downlink data frame and uplink data frame.

Frames Head started and ended with 0x7E in sender.

Byte stuffing method in sender, except the frame head, the other data must be converted when it equal 0x7E or 0x7D. 0x7E converts to 0x7D and 0x5E; 0x7D converts to 0X7D and 0x5D. In receiver, if 0x7D is received, this byte should be omitted, and next byte value should XOR or ADD with 0x20.

CRC byte this byte is summed from Len field to the byte in front of CRC with carry should be 0xFF.

Len byte the value is the number of bytes in the frame, Head/Len/CRC bytes are not included

Control Frame

Head	Len	Type	channel Frame	CRC	END
0x7E	0x19	0x00	[data1] [data2] .... [data22] [flags][RSSI]	xx	0x7E
			Same as SBUS		

Downlink Data Frame

Head	len	Type	PRIM	APPID.L	APPID.H	DATA	CRC	END
0x7E	0x08	0x01	0	0	0	0	xx	0x7E
			D0	D1	D2	D3…6	D7	

Uplink Data Frame

Len	Type	PRIM	APPID.L	APPID.H	D0	D1	D2	D3	CRC
0x08	0x81	0x00/0x10	xx	xx	xx	xx	xx	xx	xx

TYPE 0x00 control
0x01 downlink
0x81 uplink

PRIM 0x00 NULL (master/slave)

0x10 DATA	(master/slave)
0x30 READ	(master)
0x31 WRITE	(master)
0x32 RESPONSE	(slave)

APPID same as S.PORT

Channel Frame same as SBUS

DATA low byte first, 32bit in all

3. Timing

Master arranges the timing of transaction, and the action of Slave is according to the Master's arrangement.

Master sends downlink frame just after the channel frame per 9ms. Slave responds within 3ms, after the downlink frame.

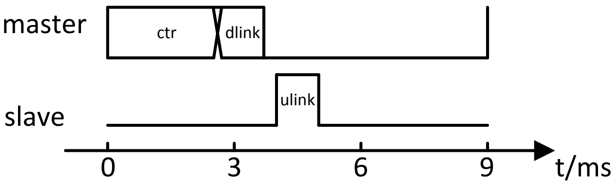

Figure 1. Timing diagram of F.Port

Ctr: control frame/dlink: down link frame by master / ulink: uplink frame by slave.

4. Communication

There are four type frames Master may send like below.

No.	Head	Length	Type	S-BUS	CRC	END
a)	0x7E	0x19	0x00	xx.....xx	xx	0x7E

No.	Head	Length	Type	Prime	APPID	DATA	CRC	END
b)	0x7E	0x08	0x01	0x00/10	xx xx	xx xx xx xx	xx	0x7E
c)	0x7E	0x08	0x01	0x30	xx xx	xx xx xx xx	xx	0x7E
d)	0x7E	0x08	0x01	0x31	xx xx	xx xx xx xx	xx	0x7E

No. a is the channel frame (generally), b, c and d are downlink frames. Master will send one of b, c or d frames just after a frame have been sent, without any delay.

There are three frames Slave may send like below.

No.	Length	Type	Prime	APPID	DATA	CRC
1)	0x08	0x81	0x00	xx xx	00 00 00 00	xx
2)	0x08	0x81	0x10	xx xx	xx xx xx xx	xx
3)	0x08	0x81	0x32	xx xx	xx xx xx xx	xx

Slave will send frame 1 or 2 if frame b has been received. If slave get ready, frame 2 will be sent, else frame 1 will be sent.

Frame 3 will be sent, if frame c or d has been received.

For example,

Master :

Head len type	d1 d2 d3 d4 d5 d6 d7 d8 d9 d10 d11 d12 d13 d14 d15 d16 d17 d18 d19 d20

7E 19 00	43 03 DE D0 D0 97 3E 56 4C 9C 15 AC 48 DF C4 93 07 3E F0 41

D21 d22 flags RSSI CRC	End Head	Len type prim appId L/H D1 D2 D3 D4 CRC END
7B E2 00 0F E2	7E 7E	08 01 00 00 00 00 00 00 00 F6 7E

Slave:

Len type prim	AppIdL AppIdH	D1 D2 D3 D4	CRC
08 81 10	00 04	2E 00 00 00	34

5. Version Record

VERSION	REMARK	Date
V1.0	Release	2017.2.17
V2.0	Drop SBUS start byte and end byte, add RSSI byte in control frame, the length byte becomes 0x19.	2017.9.18
V2.1	Fixed mistakes in protocol description.	2017.11.21